EXHIBIT 39

EXHIBIT 39

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4413A POWER MOSFET

CLAIM	AO4413A POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4413A Power MOSFET is a trenched field effect transistor. (Fig. AO4413A-1 (datasheet); Fig. AO4413A-2 (package marking).) The method used to manufacture the AO4413A power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with P-type dopants. In the language of the claim, the P-type dopants in the substrate are a "first conductivity type." (Fig. AO4413A-1 (datasheet); Fig. AO4413A-3 (Scanning Electron Microscopy image), item A; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item G; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a N-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second	The accused method includes creating a N-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the N-type doped well (the

CLAIM	AO4413A POWER MOSFET
conductivity type and forming an abrupt junction with the well;	second depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having P-type dopants (a first conductivity type). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item C; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the N-doped heavy body is created in the N-doped well includes two implants of N-type dopants (a double implant process). (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)

CLAIM	AO4413A POWER MOSFET
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the N-type heavy body is created includes a process in which N-type dopants (a second conductivity type) are diffused into the N-doped well. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with P-type dopants (a first conductivity type). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item A; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item G; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a N-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a N-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the N-type doped well (the second depth). (Fig. AO4413A-3 (Scanning Electron

CLAIM	AO4413A POWER MOSFET
	Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.)
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an P-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item C; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 40

EXHIBIT 40

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO6405 POWER MOSFET

CLAIM	AO6405 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO6405 Power MOSFET is a trenched field effect transistor. (Fig. AO6405-1 (datasheet); Fig. AO6405-2 (package marking).) The method used to manufacture the AO6405 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with P-type dopants. In the language of the claim, the P-type dopants in the substrate are a "first conductivity type." (Fig. AO6405-1 (datasheet); Fig. AO6405-3 (Scanning Electron Microscopy image), item A; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO6405-3 (Scanning Electron Microscopy image), item G; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a N-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a N-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the N-type doped well (the second depth). (Fig. AO6405-3 (Scanning Electron

CLAIM	AO6405 POWER MOSFET
well;	Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having P-type dopants (a first conductivity type). (Fig. AO6405-3 (Scanning Electron Microscopy image), item C; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the N-doped heavy body is created in the N-doped well includes two implants of N-type dopants (a double implant process). (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO6405-5 (Secondary Ion Mass

CLAIM	AO6405 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the N-type heavy body is created includes a process in which N-type dopants (a second conductivity type) are diffused into the N-doped well. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with P-type dopants (a first conductivity type). (Fig. AO6405-3 (Scanning Electron Microscopy image), item A; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO6405-3 (Scanning Electron Microscopy image), item G; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a N-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a N-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the N-type doped well (the second depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO6405 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an P-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO6405-3 (Scanning Electron Microscopy image), item C; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 41

EXHIBIT 41

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4912 POWER MOSFET

CLAIM	AO4912 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4912 Power MOSFET is a trenched field effect transistor. (Fig. AO4912-1 (datasheet); Fig. AO4912-2 (package marking).) The method used to manufacture the AO4912 Power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4912-1 (datasheet); Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4912-3 (Scanning Electron Microscopy image), item G; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4912-3 (Scanning Electron

CLAIM	AO4912 POWER MOSFET
well;	Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4912-5 (Secondary Ion Mass

CLAIM	AO4912 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.	The accused method includes patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B; Fig. AO4912-8 (Scanning Electron Microscopy image (plan view)), item B.)
16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.	The accused method includes forming a contact area on the surface of the semiconductor substrate between adjacent trenches. (Fig. AO4912-8 (Scanning Electron Microscopy image (plan view), item C; Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), item A.)
17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.	The accused method includes forming alternating source contact regions and heavy body contact regions. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)
18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.	The accused method includes forming a ladder-shaped source contact region surrounding heavy body contact regions. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)
19. The method claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:	
forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions;	The accused method includes forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), item B.)
and implanting dopants of the first conductivity type to form the ladder-shaped source contact region.	The accused method includes implanting N-type dopants (a first conductivity type) to form the ladder-shaped source contact region. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), item C.)
20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.	The accused method includes forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)

CLAIM	AO4912 POWER MOSFET
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4912-3 (Scanning Electron Microscopy image), item G; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating a N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)

CLAIM	AO4912 POWER MOSFET
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 42

EXHIBIT 42

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AOD438 POWER MOSFET

CLAIM	AOD438 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AOD438 Power MOSFET is a trenched field effect transistor. (Fig. AOD438-1 (datasheet); Fig. AOD438-2 (package marking).) The method used to manufacture the AOD438 Power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD438-1 (datasheet); Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AOD438-3 (Scanning Electron Microscopy image), item G; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOD438-3 (Scanning Electron

CLAIM	AOD438 POWER MOSFET
well;	Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level	In the accused method, the first energy level is higher than the

CLAIM	AOD438 POWER MOSFET
is higher than the second energy level.	second energy level. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.	The accused method includes patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B; Fig. AOD438-8 (Scanning Electron Microscopy image (plan view)), item B.)
16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.	The accused method includes forming a contact area on the surface of the semiconductor substrate between adjacent trenches. (Fig. AOD438-8 (Scanning Electron Microscopy image (plan view), item C; Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), item A.)
17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.	The accused method includes forming alternating source contact regions and heavy body contact regions. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)
18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.	The accused method includes forming a ladder-shaped source contact region surrounding heavy body contact regions. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)
19. The method claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:	
forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions;	The accused method includes forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), item B.)
and implanting dopants of the first conductivity type to form the ladder-shaped source contact region.	The accused method includes implanting N-type dopants (a first conductivity type) to form the ladder-shaped source contact region. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), item C.)
20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.	The accused method includes forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)

CLAIM	AOD438 POWER MOSFET
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AOD438-3 (Scanning Electron Microscopy image), item G; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating a N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)

CLAIM	AOD438 POWER MOSFET
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 43

EXHIBIT 43

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AOL1414 POWER MOSFET

CLAIM	AOL1414 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AOL1414 Power MOSFET is a trenched field effect transistor. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-2 (package marking).) The method used to manufacture the AOL1414 Power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1414-1 (datasheet); Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item G; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOL1414-3 (Scanning Electron

CLAIM	AOL1414 POWER MOSFET
well;	Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level	In the accused method, the first energy level is higher than the

CLAIM	AOL1414 POWER MOSFET
is higher than the second energy level.	second energy level. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.	The accused method includes patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B; Fig. AOL1414-8 (Scanning Electron Microscopy image (plan view)), item B.)
16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.	The accused method includes forming a contact area on the surface of the semiconductor substrate between adjacent trenches. (Fig. AOL1414-8 (Scanning Electron Microscopy image (plan view), item C; Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), item A.)
17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.	The accused method includes forming alternating source contact regions and heavy body contact regions. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)
18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.	The accused method includes forming a ladder-shaped source contact region surrounding heavy body contact regions. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)
19. The method claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:	
forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions;	The accused method includes forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), item B.)
and implanting dopants of the first conductivity type to form the ladder-shaped source contact region.	The accused method includes implanting N-type dopants (a first conductivity type) to form the ladder-shaped source contact region. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), item C.)
20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.	The accused method includes forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), items B, C.)

CLAIM	AOL1414 POWER MOSFET
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item G; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating a N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)

CLAIM	AOL1414 POWER MOSFET
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 44

EXHIBIT 44

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4812 POWER MOSFET

CLAIM	AO4812 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4812 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4812-1 (datasheet); Fig. AO4812-2 (package marking); Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4812 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4812-1 (datasheet); Fig. AO4812-3 (Scanning Electron Microscopy image), item A; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4812-3 (Scanning Electron Microscopy

CLAIM	AO4812 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4812 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO4812-1 (datasheet); Fig. AO4812-2 (package marking).) The method used to manufacture the AO4812 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4812-3 (Scanning Electron Microscopy image), item F; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4812-3 (Scanning Electron Microscopy image), item G; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO4812 POWER MOSFET
	dielectric-lined trenches. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4812-3 (Scanning Electron Microscopy image), item C; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4812-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4812-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect	The accused method includes the creation of a field

CLAIM	AO4812 POWER MOSFET
transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	termination structure around the periphery of the field effect transistor. (Fig. AO4812-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 45

EXHIBIT 45

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4468 POWER MOSFET

CLAIM	AO4468 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4468 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4468-1 (datasheet); Fig. AO4468-2 (package marking); Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4468 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4468-1 (datasheet); Fig. AO4468-3 (Scanning Electron Microscopy image), item A; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4468-3 (Scanning Electron Microscopy

CLAIM	AO4468 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4468 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO4468-1 (datasheet); Fig. AO4468-2 (package marking).) The method used to manufacture the AO4468 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4468-3 (Scanning Electron Microscopy image), item F; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4468-3 (Scanning Electron Microscopy image), item G; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO4468 POWER MOSFET
	dielectric-lined trenches. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4468-3 (Scanning Electron Microscopy image), item C; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4468-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4468-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect	The accused method includes the creation of a field

CLAIM	AO4468 POWER MOSFET
transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	termination structure around the periphery of the field effect transistor. (Fig. AO4468-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 46

EXHIBIT 46

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO6402 POWER MOSFET

CLAIM	AO6402 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO6402 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO6402-1 (datasheet); Fig. AO6402-2 (package marking); Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO6402 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO6402-1 (datasheet); Fig. AO6402-3 (Scanning Electron Microscopy image), item A; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO6402-3 (Scanning Electron Microscopy

CLAIM	AO6402 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO6402 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO6402-1 (datasheet); Fig. AO6402-2 (package marking).) The method used to manufacture the AO6402 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO6402-3 (Scanning Electron Microscopy image), item F; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO6402-3 (Scanning Electron Microscopy image), item G; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO6402 POWER MOSFET
	dielectric-lined trenches. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO6402-3 (Scanning Electron Microscopy image), item C; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO6402-3 (Scanning Electron Microscopy image), items C, E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO6402-3 (Scanning Electron Microscopy image), items C, E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect	The accused method includes the creation of a field

CLAIM	AO6402 POWER MOSFET
transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	termination structure around the periphery of the field effect transistor. (Fig. AO6402-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 47

EXHIBIT 47

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AOL1412 POWER MOSFET

CLAIM	AOL1412 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AOL1412 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AOL1412-1 (datasheet); Fig. AOL1412-2 (package marking); Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AOL1412 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AOL1412-1 (datasheet); Fig. AOL1412-3 (Scanning Electron Microscopy image), item A; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AOL1412-3 (Scanning Electron

CLAIM	AOL1412 POWER MOSFET
that is greater than said dosage of said third dopant.	Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AOL1412 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AOL1412-1 (datasheet); Fig. AOL1412-2 (package marking).) The method used to manufacture the AOL1412 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item F; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item G; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item G.)

CLAIM	AOL1412 POWER MOSFET
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the dielectric-lined trenches. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item C; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOL1412-3 (Scanning Electron Microscopy image), items C, E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOL1412-3 (Scanning Electron Microscopy image), items C, E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.

CLAIM	AOL1412 POWER MOSFET
13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	The accused method includes the creation of a field termination structure around the periphery of the field effect transistor. (Fig. AOL1412-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 48

EXHIBIT 48

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4410 POWER MOSFET

CLAIM	AO4410 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4410 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4410-1 (datasheet); Fig. AO4410-2 (package marking); Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4410 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4410-1 (datasheet); Fig. AO4410-3 (Scanning Electron Microscopy image), item A; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4410-3 (Scanning Electron Microscopy

CLAIM	AO4410 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4410 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO4410-1 (datasheet); Fig. AO4410-2 (package marking).) The method used to manufacture the AO4410 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4410-3 (Scanning Electron Microscopy image), item F; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4410-3 (Scanning Electron Microscopy image), item G; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO4410 POWER MOSFET
	dielectric-lined trenches. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4410-3 (Scanning Electron Microscopy image), item C; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4410-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4410-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect	The accused method includes the creation of a field

CLAIM	AO4410 POWER MOSFET
transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	termination structure around the periphery of the field effect transistor. (Fig. AO4410-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 49

EXHIBIT 49

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4914 POWER MOSFET

CLAIM	AO4914 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4914 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4914-1 (datasheet); Fig. AO4914-2 (package marking); Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4914 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4914-1 (datasheet); Fig. AO4914-3 (Scanning Electron Microscopy image), item A; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4914-3 (Scanning Electron Microscopy

CLAIM	AO4914 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4914 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO4914-1 (datasheet); Fig. AO4914-2 (package marking).) The method used to manufacture the AO4914 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4914-3 (Scanning Electron Microscopy image), item F; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4914-3 (Scanning Electron Microscopy image), item G; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO4914 POWER MOSFET
	dielectric-lined trenches. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4914-3 (Scanning Electron Microscopy image), item C; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4914-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4914-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect	The accused method includes the creation of a field

CLAIM	AO4914 POWER MOSFET
transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	termination structure around the periphery of the field effect transistor. (Fig. AO4914-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 50

EXHIBIT 50

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4422 POWER MOSFET

CLAIM	AO4422 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4422 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4422-1 (datasheet); Fig. AO4422-2 (package marking); Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4422 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4422-1 (datasheet); Fig. AO4422-3 (Scanning Electron Microscopy image), item A; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4422-3 (Scanning Electron Microscopy

CLAIM	AO4422 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4422 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO4422-1 (datasheet); Fig. AO4422-2 (package marking).) The method used to manufacture the AO4422 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4422-3 (Scanning Electron Microscopy image), item F; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4422-3 (Scanning Electron Microscopy image), item G; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO4422 POWER MOSFET
	dielectric-lined trenches. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4422-3 (Scanning Electron Microscopy image), item C; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4422-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4422-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect	The accused method includes the creation of a field

CLAIM	AO4422 POWER MOSFET
transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	termination structure around the periphery of the field effect transistor. (Fig. AO4422-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 51

EXHIBIT 51

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4704 POWER MOSFET

CLAIM	AO4704 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4704 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4704-1 (datasheet); Fig. AO4704-2 (package marking); Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4704 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4704-1 (datasheet); Fig. AO4704-3 (Scanning Electron Microscopy image), item A; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4704-3 (Scanning Electron Microscopy

CLAIM	AO4704 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4704 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO4704-1 (datasheet); Fig. AO4704-2 (package marking).) The method used to manufacture the AO4704 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4704-3 (Scanning Electron Microscopy image), item F; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4704-3 (Scanning Electron Microscopy image), item G; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO4704 POWER MOSFET
	dielectric-lined trenches. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4704-3 (Scanning Electron Microscopy image), item C; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4704-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4704-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect	The accused method includes the creation of a field

CLAIM	AO4704 POWER MOSFET
transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	termination structure around the periphery of the field effect transistor. (Fig. AO4704-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 52

EXHIBIT 52

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AOD414 POWER MOSFET

CLAIM	AOD414 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AOD414 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AOD414-1 (datasheet); Fig. AOD414-2 (package marking); Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AOD414 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AOD414-1 (datasheet); Fig. AOD414-3 (Scanning Electron Microscopy image), item A; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AOD414-3 (Scanning Electron

CLAIM	AOD414 POWER MOSFET
that is greater than said dosage of said third dopant.	Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AOD414 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AOD414-1 (datasheet); Fig. AOD414-2 (package marking).) The method used to manufacture the AOD414 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AOD414-3 (Scanning Electron Microscopy image), item F; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AOD414-3 (Scanning Electron Microscopy image), item G; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item G.)

CLAIM	AOD414 POWER MOSFET
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the dielectric-lined trenches. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AOD414-3 (Scanning Electron Microscopy image), item C; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOD414-3 (Scanning Electron Microscopy image), items C, E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOD414-3 (Scanning Electron Microscopy image), items C, E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.

CLAIM	AOD414 POWER MOSFET
13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	The accused method includes the creation of a field termination structure around the periphery of the field effect transistor. (Fig. AOD414-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 53

EXHIBIT 53

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4413A POWER MOSFET

CLAIM	AO4413A POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4413A Power MOSFET is a P-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4413A-1 (datasheet); Fig. AO4413A-2 (package marking); Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4413A power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4413A-1 (datasheet); Fig. AO4413A-3 (Scanning Electron Microscopy image), item A; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a N-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a N-type dopant (second dopant) at a second energy and dosage. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a N-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4413A-3 (Scanning Electron

CLAIM	AO4413A POWER MOSFET
that is greater than said dosage of said third dopant.	Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).))
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4413A Power MOSFET is a P-channel trenched field effect transistor. (Fig. AO4413A-1 (datasheet); Fig. AO4413A-2 (package marking).) The method used to manufacture the AO4413A Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item F; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item G; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the dielectric-lined trenches. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)

CLAIM	AO4413A POWER MOSFET
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an P-type dopant (a first type). Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (a second type opposite the first type (P-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (a type opposite the first type (P-type)) in regions between adjacent trenches to form a plurality of N-type doped heavy bodies within the wells, and N-type doped contact areas. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item C; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a N-type dopant (first dopant) at a first energy and dosage and a N-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4413A-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4413A-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	The accused method includes the creation of a field termination structure around the periphery of the field effect transistor. (Fig. AO4413A-6 (Scanning Electron Microscopy), item A.)

CLAIM	AO4413A POWER MOSFET
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and N-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and N-type doped contact areas. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.)
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 54

EXHIBIT 54

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO6405 POWER MOSFET

CLAIM	AO6405 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO6405 Power MOSFET is a P-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO6405-1 (datasheet); Fig. AO6405-2 (package marking); Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO6405 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO6405-1 (datasheet); Fig. AO6405-3 (Scanning Electron Microscopy image), item A; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a N-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a N-type dopant (second dopant) at a second energy and dosage. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a N-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO6405-3 (Scanning Electron Microscopy

CLAIM	AO6405 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).))
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO6405 Power MOSFET is a P-channel trenched field effect transistor. (Fig. AO6405-1 (datasheet); Fig. AO6405-2 (package marking).) The method used to manufacture the AO6405 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO6405-3 (Scanning Electron Microscopy image), item F; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO6405-3 (Scanning Electron Microscopy image), item G; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the dielectric-lined trenches. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an

CLAIM	AO6405 POWER MOSFET
	P-type dopant (a first type). Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (a second type opposite the first type (P-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (a type opposite the first type (P-type)) in regions between adjacent trenches to form a plurality of N-type doped heavy bodies within the wells, and N-type doped contact areas. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO6405-3 (Scanning Electron Microscopy image), item C; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a N-type dopant (first dopant) at a first energy and dosage and a N-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO6405-3 (Scanning Electron Microscopy image), items C, E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO6405-3 (Scanning Electron Microscopy image), items C, E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	The accused method includes the creation of a field termination structure around the periphery of the field effect transistor. (Fig. AO6405-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect	The accused method includes the deposition of a dielectric

CLAIM	AO6405 POWER MOSFET
transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	layer prior to the creation of the heavy bodies and N-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and N-type doped contact areas. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.)
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 55

EXHIBIT 55

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AO4912 POWER MOSFET

CLAIM	AO4912 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AO4912 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AO4912-1 (datasheet); Fig. AO4912-2 (package marking); Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AO4912 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AO4912-1 (datasheet); Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AO4912-3 (Scanning Electron Microscopy

CLAIM	AO4912 POWER MOSFET
that is greater than said dosage of said third dopant.	image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AO4912 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AO4912-1 (datasheet); Fig. AO4912-2 (package marking).) The method used to manufacture the AO4912 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item F; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AO4912-3 (Scanning Electron Microscopy image), item G; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item G.)
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the

CLAIM	AO4912 POWER MOSFET
	dielectric-lined trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
8. The method of manufacturing a trenched field effect transistor of claim 7 wherein the trenches are patterned to extend in one direction and be substantially parallel to each other.	The accused method includes the step of forming trenches that are patterned to extend in one direction and be substantially parallel to each other. (Fig. AO4912-6 (Scanning Electron Microscopy image (plan view)), item B; Fig. AO4912-8 (Scanning Electron Microscopy image (plan view)), item B.)
9. The method of manufacturing a trenched field effect transistor of claim 7 wherein the patterning and implanting steps further comprise arranging the first dopant type contact areas and second dopant type contact areas in alternation and extend linearly between adjacent trenches.	The accused method includes the step of forming N-type (first type) dopant contact areas and P-type (second type) dopant contact areas in alternation and extending linearly between adjacent trenches. (Fig. AO4912-8 (Scanning Electron Microscopy image (plan view)), items B, C.)

CLAIM	AO4912 POWER MOSFET
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4912-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AO4912-3 (Scanning Electron Microscopy image), items C, E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	The accused method includes the creation of a field termination structure around the periphery of the field effect transistor. (Fig. AO4912-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 56

EXHIBIT 56

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AOD438 POWER MOSFET

CLAIM	AOD438 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AOD438 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AOD438-1 (datasheet); Fig. AOD438-2 (package marking); Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AOD438 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AOD438-1 (datasheet); Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AOD438-3 (Scanning Electron

CLAIM	AOD438 POWER MOSFET
that is greater than said dosage of said third dopant.	Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AOD438 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AOD438-1 (datasheet); Fig. AOD438-2 (package marking).) The method used to manufacture the AOD438 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item F; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AOD438-3 (Scanning Electron Microscopy image), item G; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item G.)

CLAIM	AOD438 POWER MOSFET
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the dielectric-lined trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
8. The method of manufacturing a trenched field effect transistor of claim 7 wherein the trenches are patterned to extend in one direction and be substantially parallel to each other.	The accused method includes the step of forming trenches that are patterned to extend in one direction and be substantially parallel to each other. (Fig. AOD438-6 (Scanning Electron Microscopy image (plan view)), item B; Fig. AOD438-8 (Scanning Electron Microscopy image (plan view)), item B.)
9. The method of manufacturing a trenched field effect transistor of claim 7 wherein the patterning and implanting steps further comprise arranging the first dopant type contact areas and second dopant type contact areas in alternation and extend linearly between adjacent	The accused method includes the step of forming N-type (first type) dopant contact areas and P-type (second type) dopant contact areas in alternation and extending linearly between adjacent trenches. (Fig. AOD438-8 (Scanning Electron Microscopy image (plan view)), items B, C.)

CLAIM	AOD438 POWER MOSFET
trenches.	
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOD438-3 (Scanning Electron Microscopy image), items C, E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOD438-3 (Scanning Electron Microscopy image), items C, E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	The accused method includes the creation of a field termination structure around the periphery of the field effect transistor. (Fig. AOD438-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).))

EXHIBIT 57

EXHIBIT 57

INFRINGEMENT OF U.S. PATENT NO. 6,521,497

AOS AOL1414 POWER MOSFET

CLAIM	AOL1414 POWER MOSFET
1. A method of making a heavy body structure for a trenched DMOS transistor comprising:	The AOS AOL1414 Power MOSFET is an N-channel trenched double-Diffused Metal Oxide Semiconductor (DMOS) transistor that contains a heavy body structure. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-2 (package marking); Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.) The method used to create the heavy body structure for the AOL1414 power MOSFET is, by definition, a method of manufacturing a heavy body structure for a trenched DMOS transistor (the "accused method").
providing a semiconductor substrate;	The accused method includes the use of a semiconductor substrate. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches into the substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;	The accused method includes creating a doped well by implanting a P-type dopant (first dopant), at a first energy and dosage, into the semiconductor substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body;	The accused method includes creating a first doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (second dopant) at a second energy and dosage. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
and implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body, wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration	The accused method includes creating a second doped portion of a heavy body, between adjacent trenches, by implanting into the doped well a P-type dopant (third dopant) at a third energy and dosage. The dosage of the second dopant has a doping concentration that is greater than the dosage of the third dopant. (Fig. AOL1414-3 (Scanning Electron

CLAIM	AOL1414 POWER MOSFET
that is greater than said dosage of said third dopant.	Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).))
2. The method of claim 1 wherein said first and second dopants both comprise boron.	Because the accused method fabricates an N-channel device, the first and second dopants are boron. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.	On information and belief, the first energy in the accused method is from about 30 to 100 keV. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
4. The method of claim 3 wherein said first dosage is from about 1E13 to 1E15 cm.sup.-2.	On information and belief, the first dosage in the accused method is from about 1E13 to 1E15 cm.sup.-2. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.	On information and belief, the second energy in the accused method is from about 150 to 200 keV. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E).)
6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm.sup.-2.	On information and belief, the second dosage in the accused method is from about 1E15 to 5E15 cm.sup.-2. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E).)
7. A method of manufacturing a trenched field effect transistor comprising:	The AOS AOL1414 Power MOSFET is an N-channel trenched field effect transistor. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-2 (package marking).) The method used to manufacture the AOL1414 Power MOSFET is, by definition, a method of manufacturing a trenched field effect transistor (the "accused method").
forming an epitaxial layer on a semiconductor substrate;	The accused method includes creating an epitaxial layer on the semiconductor substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item F; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item F).)
patterning and etching a plurality of trenches into the epitaxial layer;	The accused method includes patterning and etching a plurality of trenches into the semiconductor substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B).)
lining each trench with a gate dielectric layer;	The accused method includes lining each trench with a gate dielectric layer. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item G; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item G.)

CLAIM	AOL1414 POWER MOSFET
depositing polysilicon to fill the dielectric-lined trenches;	The accused method includes depositing polysilicon to fill the dielectric-lined trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
doping the polysilicon with a dopant of a first type;	The accused method includes doping the polysilicon with an N-type dopant (a first type). Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B).)
patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a second type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of doped wells interposed between adjacent trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;	The accused method includes patterning the epitaxial layer and implanting a P-type dopant (a type opposite the first type (N-type)) in regions between adjacent trenches to form a plurality of P-type doped heavy bodies within the wells, and P-type doped contact areas. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas;	The accused method includes patterning the epitaxial layer and implanting a N-type dopant (first type) to form doped source regions and doped contact areas. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C.)
and applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.	The accused method includes depositing a dielectric on the surface of the semiconductor substrate and patterning the dielectric to expose contact areas. The implanting step for forming the heavy bodies includes implanting a P-type dopant (first dopant) at a first energy and dosage and a P-type dopant (second dopant) at a second energy and dosage, wherein the second energy and dosage is less than the first energy and dosage. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
8. The method of manufacturing a trenched field effect transistor of claim 7 wherein the trenches are patterned to extend in one direction and be substantially parallel to each other.	The accused method includes the step of forming trenches that are patterned to extend in one direction and be substantially parallel to each other. (Fig. AOL1414-6 (Scanning Electron Microscopy image (plan view)), item B; Fig. AOL1414-8 (Scanning Electron Microscopy image (plan view)), item B.)
9. The method of manufacturing a trenched field effect transistor of claim 7 wherein the patterning and implanting steps further comprise arranging the first dopant type contact areas and second dopant type contact areas in alternation and extend linearly between adjacent	The accused method includes the step of forming N-type (first type) dopant contact areas and P-type (second type) dopant contact areas in alternation and extending linearly between adjacent trenches. (Fig. AOL1414-8 (Scanning Electron Microscopy image (plan view)), items B, C.)

CLAIM	AOL1414 POWER MOSFET
trenches.	
11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items C, E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items C, E.) If ***before***, this step is practiced.
12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.	In the accused method, the doped heavy bodies are formed before or after the formation of the source regions. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items C, E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items C, E.) If ***after***, this step is practiced.
13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.	The accused method includes the creation of a field termination structure around the periphery of the field effect transistor. (Fig. AOL1414-6 (Scanning Electron Microscopy), item A.)
15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.	The accused method includes the deposition of a dielectric layer prior to the creation of the heavy bodies and P-type doped contact areas, thus creating a mask of dielectric used in the creation of the heavy bodies and P-type doped contact areas. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm.sup.-2.	The third dopant in the accused method includes boron and, on information and belief, the third dosage is from about 1E14 to 1E15cm.sup.-2. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).))
17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.	On information and belief, the third energy in the accused method is from about 20 to 40 keV. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).))